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EXAMINER	
CHEN, CHIA WEI A	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,440	ALTICE, PETER PARKER	
	Examiner	Art Unit	
	Chia-Wei A. Chen	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 11, 33, 24, 25, and 36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 6, 9, 10-12, 14, 16, 19, 20, 21-23, 25, 27-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1).

As to claim 1, Weale discloses, in Figure 1, a pixel cell, comprising:

- a first storage node (120) for storing charge generated at a photosensitive element (112) during an integration period; and
- a second storage node (140) for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node (col. 3, lines 42-53),

but does not teach wherein the charges are stored prior to storing said charge at a floating diffusion region.

Guidash teaches, in Figure 1b and 2, transferring charges to a floating diffusion region (18) (col. 4, lines 17-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the structure of the pixel cell, specifically the floating diffusion region of Guidash, with the dual storage node pixel cell of Weale in order to provide extended dynamic range and high sensitivity to incident light. (See col. 2, lines 6-9 of Guidash.)

As to claim 2, Weale wherein said photosensitive element is a photodiode (112; col. 4, line 29).

As to claim 4, Weale teaches wherein said first storage node comprises a storage capacitor (122; col. 3, line 67).

As to claim 6, Weale teaches wherein said second storage node comprises a storage capacitor (142; col. 4, line 3).

As to claim 9, Weale teaches, in Figure 1, a pixel cell further comprising a first transfer transistor (162) switchably coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 4, lines 34-41).

As to claim 10, Weale teaches, in Figure 5, a pixel cell further comprising:

- a first transfer transistor (262) switchably coupled between said first storage node and said floating diffusion region; and
- a second transfer transistor (272) switchably coupled between said second storage node and said floating diffusion region (col. 11, lines 33-40).

As to claims 11, 12, 14, 16, 19, and 20, these claims only differ from claims 1, 2, 4, 6, 9, and 10 in that claims 11, 12, 14, 16, 19, and 20 claim a semiconductor chip comprising a plurality of pixels (Weale discloses a pixel array (col. 19, line 52) and a semiconductor chip (col. 5, lines 53-54)), each pixel having the same configuration as claimed in claims 1, 2, 4, 6, 9, and 10. Thus, claims 11, 12, 14, 16, 19, and 20 are analyzed as previously discussed in claims 1, 2, 4, 6, 9, and 10.

As to claim 21, Guidash teaches the chip further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region (Fig. 1B, col. 3, line 62-col. 4, line 13).

As to claim 22, Guidash teaches wherein said sample and hold circuit comprises at least four storage nodes, each respectively for storing a reset voltage and a signal voltage representing a charge stored by each of said first and second storage nodes (C5 and C6, Fig. 1b of Guidash, col. 4, lines 46-51). (It would have been obvious to one

skilled in the art to have used a sample and hold circuit, as taught by Guidash, for each of the storage nodes, as taught in Weale.)

As to claim 23, Guidash teaches wherein said sample and hold circuit further comprises at least two storage nodes (C5 and C6 of Guidash) for respectively storing a reset voltage of said floating diffusion region and a signal voltage of at least one of said first and second storage nodes (col. 4, lines 46-51).

As to claim 25, Weale teaches, in Figure 1, a method for operating an image sensor, the method comprising:

- receiving, at a first storage node (120) of a pixel cell, charge generated by a photosensitive element (112) of said pixel cell during an integration period (col. 3, lines 42-53);
- receiving, at a second storage node (140) of said pixel cell, a portion of said charge generated by said photosensitive element during the integration period not stored at said first storage node (col. 3, lines 42-53);

Guidash teaches

- transferring said charge from to a floating diffusion region (18) of said pixel cell (col. 4, lines 17-20 of Guidash).

As to claim 27, Weale teaches wherein said second act of receiving comprises receiving said portion of said charge at a storage capacitor (142) of said pixel cell (col. 4, line 3).

As to claim 28, Weale teaches wherein said act of transferring comprises:

- transferring said charge from said first storage node (120) (col. 3, lines 51-53) and to a column line associated with said pixel cell (Fig. 1; output is readout to the column bus);

Guidash teaches;

- transferring charges to a floating diffusion region (col. 2, lines 6-9).

As to claim 29, Weale teaches wherein said act of transferring comprises:

- transferring said charge from said second storage node (140) (col. 3, lines 51-53) and to a column line associated with said pixel cell (Fig. 1; output is readout to the column bus);

Guidash teaches;

- transferring charges to a floating diffusion region (col. 2, lines 6-9).

As to claim 30, Weale teaches wherein said first act of receiving comprises activating a shutter gate transistor (first charge transfer gate 124) coupled between said first storage node and said photosensitive element (Fig. 1, col. 3, line 67-col. 4, line 2).

As to claim 31, Weale teaches wherein said second act of receiving comprises activating a shutter gate transistor (second charge transfer gate 144) coupled between

said -second storage node and said photosensitive element (Fig. 1, col. 3, line 67-col. 4, 2).

As to claim 32, Weale teaches wherein said act of transferring comprises activating a transfer transistor (buffer 162) coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 4, lines 34-41).

As to claim 33, Weale teaches a method for operating an image sensor, the method comprising:

- receiving light at a photosensitive element (112) of a first pixel cell during an integration period (col. 4, lines 44-45);
- transferring charge generated during the integration period by said photosensitive element to a first storage node (120) of said first pixel cell;
- transferring a portion of said charge generated during the integration period not transferred to said first storage node to a second storage node (140) of said first pixel cell (col. 3, lines 42-53);
- transferring said charge from said first storage node to an output (col. 4, lines 34-41);
- transferring said charge from said second storage node to an output (col. 4, lines 34-41); and
- reading out said charge (output buffer 162 to column bus 166; Fig. 1);

Guidash teaches

- transferring charges to a floating diffusion region (18) of said first pixel cell (col. 4, lines 17-20);
- reading out said charge from said floating diffusion region (Charge on the floating diffusion is sampled; col. 4, lines 41-44);

As to claim 34, Weale teaches the method of claim 33 further comprising the act of resetting at least one of said photosensitive element and said floating diffusion region (preset gate 116; col. 7, lines 30-39).

4. Claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) as applied to claims 1, 11, and 25 above, and further in view of Merrill (US 6,069,376).

As to claim 3, Weale in view of Guidash teaches the pixel cell of claim 1, but does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the pixel of Weale in view of Guidash to provide a storeage-pixel sensor and an imaging array of storage-pixel sensors that incorporate a "film-speed" switching capability

without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 5, Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7).

As to claim 7, Merrill teaches wherein said gated storage node comprises (86):

- a depletion area (130) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60); and
- a barrier region (126) adjacent to said depletion area (col. 7, lines 54-56).

As to claim 8, Merrill teaches wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60).

As to claims 13, 15, 17, and 18, these claims differ only in that these claims claim a semiconductor chip comprising a plurality of pixels (Weale discloses a pixel array (col. 19, line 52) and a semiconductor chip (col. 5, lines 53-54)), each pixel having the same configuration as claimed in claims 3, 5, 7, and 8. Thus, claims 13, 15, 17, and 18 are analyzed as previously discussed in claims 3, 5, 7, and 8.

As to claim 26, Merrill teaches wherein said first act of receiving comprises receiving said charge at a gated storage node (86) of said pixel cell (col. 7, line 7).

5. Claims 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,160,281).

As to claim 24, Weale teaches a semiconductor chip (col. 5, lines 53-54), comprising:

- a plurality of pixel cells (col. 19, line 52) comprising:
- a first storage node (120) for storing charge generated at a photosensitive element (112) during an integration period prior to storing said charge on said common floating diffusion region; and
- a second storage node (140) for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node (col. 3, lines 47-51);
- but does not teach wherein at least two of which share a common floating diffusion region.

Guidash teaches wherein at least two of which share a common floating diffusion region (84; Fig. 8, col. 4, lines 57-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have have used the common floating diffusion region of Guidash with the semiconductor chip of Weale so that layout efficiencies can be utilized to improve the fill factor of the pixel. (See col. 3, lines 1-3 of Guidash (US 6,160,281).)

As to claim 35, Weale teaches the method of claim 33 further comprising:

- receiving light at a second photosensitive element (112) of a second pixel cell (col. 4, lines 44-45);
- transferring charge generated by said second photosensitive element to a first storage node (120) of said second pixel cell;
- transferring a portion of said charge not transferred to said first storage node of said second pixel cell to a second storage node (140) of said second pixel cell (col. 3, lines 42-53);
- transferring said charge from said first storage node of said second pixel cell to an output (col. 4, lines 34-41);
- transferring said charge from said second storage node of said second pixel cell to an output (col. 4, lines 34-41); and
- reading out said charge (output buffer 162 to column bus 166; Fig. 1;

Guidash teaches wherein said first and second pixel cells share said floating diffusion region (84; Fig. 8, col. 4, lines 57-61) and wherein charges are readout from said floating diffusion region (col. 5, lines 1-11).

6. Claims 36, 37, 39, 41, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) and further in view of Miyamoto (US 2003/0090575 A1).

As to claims 36, 37, 39, 41, 44, and 45, these claims differ from claims 1, 2, 4, 6, 9, and 10 only in that a processor is additionally recited. Weale as modified by Guidash does not teach a processor. Miyamoto teaches a processor (7; paragraph [0029]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the processor of Miyamoto with the system of Weale as modified by Guidash to provide an electronic still camera which is capable of effecting continuous shooting at a higher speed, which does not produce a large number of useless exposures during recording, and which is capable of reproducing an image so that the motion of a subject can be easily grasped. (See paragraph [0011] of Miyamoto).

7. Claims 38, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US 7,286,174 B1) in view of Guidash (US 6,710,804 B1) as modified by Miyamoto (US 2003/0090575 A1) as applied to claim 36 above, and further in view of Merrill (US 6,069,376).

As to claim 38, Weale in view Guidash as modified by Miyamoto does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the

pixel of Weale to provide a storeage-pixel sensor and an imaging array of storage-pixel sensors that incorporate a "film-speed" switching capability without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 40, Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7 of Merrill).

As to claim 42, Merrill teaches wherein said gated storage node comprises (86 of Merrill):

- a depletion area (130 of Merrill) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60 of Merrill); and
- a barrier region (126 of Merrill) adjacent to said depletion area (col. 7, lines 54-56 of Merrill).

As to claim 43, Merrill teaches wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60 of Merrill).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chia-Wei A. Chen whose telephone number is 571-270-1707. The examiner can normally be reached on Monday - Friday, 7:30 - 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cac
1/22/08

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER